

WHAT IS CLAIMED IS:

1. A multiplexer cell layout structure comprising:
cell arrays composed of P-channel transistors and N-channel transistors which are arranged in two upper and
5 lower rows; and
a wiring layer composed of a plurality of layers for connecting said cell arrays, in which
each of said cell arrays comprises a plurality of transfer gates, wherein
10 a plurality of transistors of said transfer gates are arranged in upper one of said cell arrays and lower one of said cell arrays, and an output terminal of the plurality of arranged transistors is connected across between said upper and lower cell arrays by 2-layer metal wiring of said wiring
15 layer.
2. The multiplexer cell layout structure as set forth in Claim 1, wherein said multiplexer has a decoding circuit which has transistors arranged on the upper side and lower side of said cell arrays.
- 20 3. The multiplexer cell layout structure as set forth in Claim 2, wherein an internal wiring of said decoding circuit is connected across between the upper and lower cell arrays by at least a wiring layer including a polysilicon layer out of said wiring layer, and a control signal wiring
25 for controlling transistor output of said transfer gate circuit is connected across between the upper and lower cell arrays by at least a wiring layer including a polysilicon layer out of said wiring layer.

4. The multiplexer cell layout structure as set forth in Claim 2, wherein internal wiring of said decoding circuit is connected by at least one of 1-layer metal wiring and 2-layer metal wiring.

5 5. The multiplexer cell layout structure as set forth in Claim 2, wherein

the control signal wiring for controlling transistor output of said transfer gate circuit is connected by 1-layer metal wiring and 2-layer metal wiring, respectively.

10 6. The multiplexer cell layout structure as set forth in Claim 1, wherein

said multiplexer cells are formed as a 4-input multiplexer-inverter.

15 7. The multiplexer cell layout structure as set forth in Claim 1, wherein

said multiplexer cells are formed as a 3-input multiplexer-inverter.

20 8. The multiplexer cell layout structure as set forth in Claim 1, wherein

said cell arrays are arranged up and down in three rows in place of two upper and lower rows.

9. The multiplexer cell layout structure as set forth in Claim 1, wherein

25 said multiplexer cells are formed as a 5-input multiplexer-inverter.

10. The multiplexer cell layout structure as set forth in Claim 1, wherein

said multiplexer cell layout structure is applied to a

barrel shifter circuit of a CPU core.